

74LVT125; 74LVTH125

3.3 V quad buffer; 3-state

Rev. 8 — 18 August 2021

Product data sheet

1. General description

The 74LVT125; 74LVTH125 is a quad buffer/line driver with 3-state outputs controlled by the output enable inputs ($n\overline{OE}$). A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Quad bus interface
- 3-state buffers
- Wide supply voltage range from 2.7 to 3.6 V
- BiCMOS high speed and output drive
- Output capability: +64 mA and -32 mA
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standard JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM EIA/JESD22-A114-A exceeds 2000V
 - MM EIA/JESD22-A115-A exceeds 200V
- Specified from -40 °C to 85 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74LVT125D | -40 °C to +85 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74LVTH125D | | | | |
| 74LVT125PW | -40 °C to +85 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74LVTH125PW | | | | |
| 74LVT125BQ | -40 °C to +85 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |
| 74LVTH125BQ | | | | |

4. Functional diagram

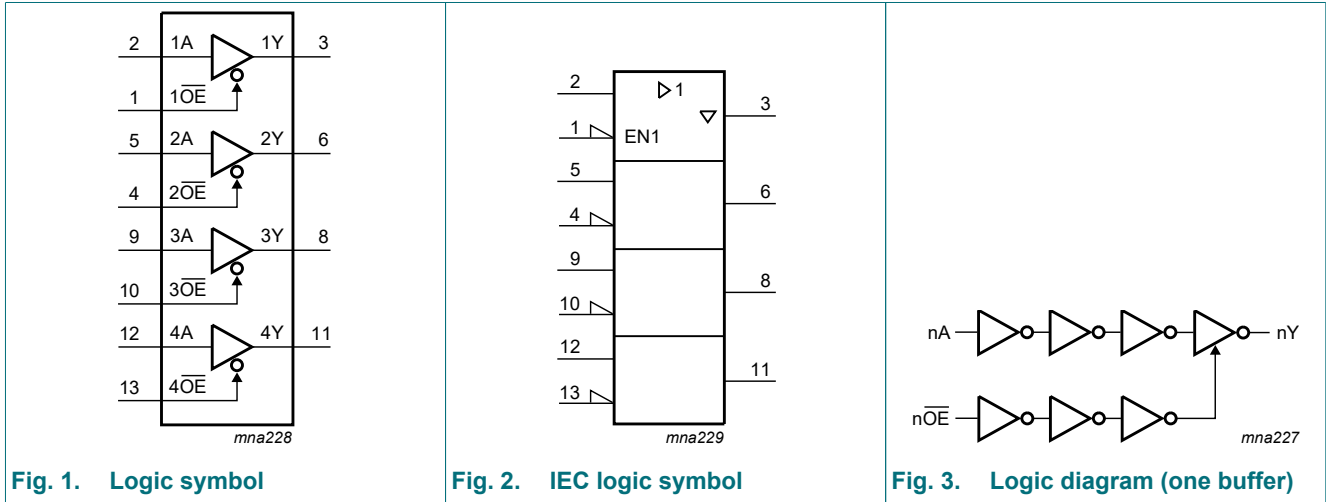


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

Fig. 3. Logic diagram (one buffer)

5. Pinning information

5.1. Pinning

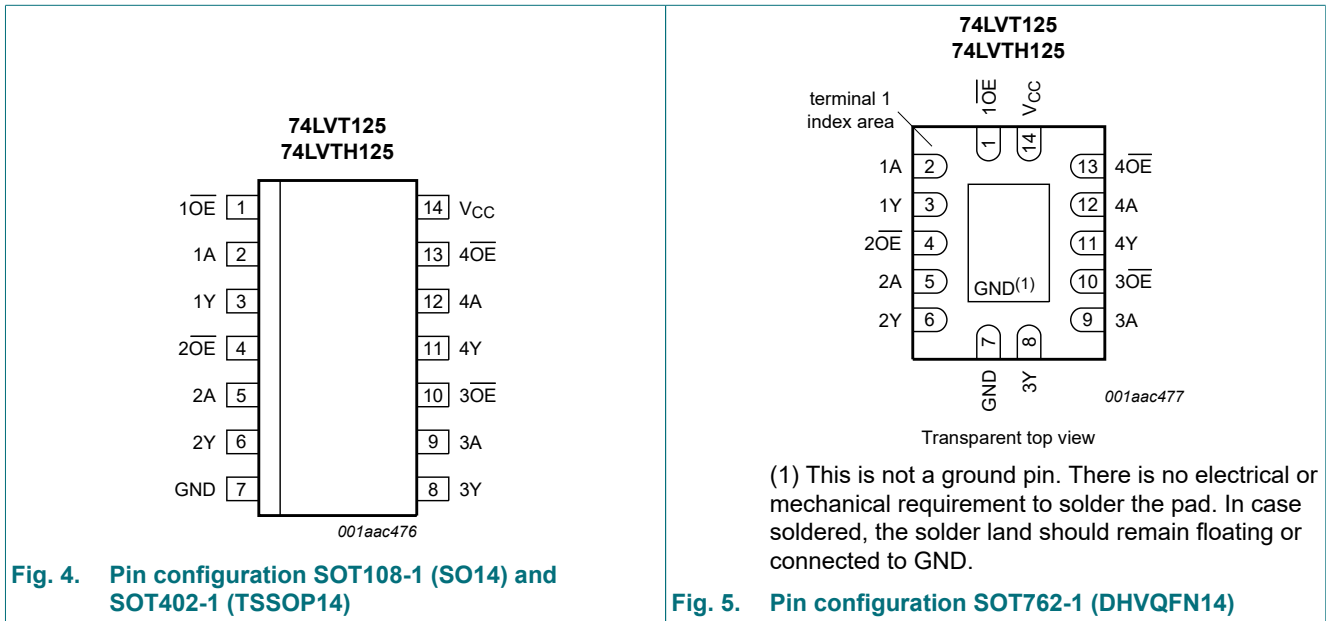


Fig. 4. Pin configuration SOT108-1 (SO14) and SOT402-1 (TSSOP14)

Fig. 5. Pin configuration SOT762-1 (DHVQFN14)

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------------------------|-----|------------------------------------|
| 1 $\overline{\text{OE}}$ | 1 | 1 output enable input (active LOW) |
| 1A | 2 | 1 data input |
| 1Y | 3 | 1 data output |
| 2 $\overline{\text{OE}}$ | 4 | 2 output enable input (active LOW) |
| 2A | 5 | 2 data input |
| 2Y | 6 | 2 data output |
| GND | 7 | ground (0 V) |
| 3Y | 8 | 3 data output |
| 3A | 9 | 3 data input |
| 3 $\overline{\text{OE}}$ | 10 | 3 output enable input (active LOW) |
| 4Y | 11 | 4 data output |
| 4A | 12 | 4 data input |
| 4 $\overline{\text{OE}}$ | 13 | 4 output enable input (active LOW) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

| Control | Input | Output |
|--------------------------|-------|--------|
| n $\overline{\text{OE}}$ | nA | nY |
| L | L | L |
| L | H | H |
| H | X | Z |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---------------------------------------|------|------|------|
| V_{CC} | supply voltage | | -0.5 | +4.6 | V |
| V_I | input voltage | [1] | -0.5 | +7.0 | V |
| V_O | output voltage | output in OFF-state or HIGH-state [1] | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | - | -50 | mA |
| I_{OK} | output clamping current | $V_O < 0$ V | - | -50 | mA |
| I_O | output current | output in LOW-state | - | 128 | mA |
| | | output in HIGH-state | - | -64 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| T_j | junction temperature | [2] | - | 150 | °C |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|---|-----|-----|-----|------|
| V_{CC} | supply voltage | | 2.7 | - | 3.6 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| I_{OH} | HIGH-level output current | | - | - | -32 | mA |
| I_{OL} | LOW-level output current | none | - | - | 32 | mA |
| | | current duty cycle $\leq 50\%$; $f \geq 1$ kHz | - | - | 64 | mA |
| $\Delta t/\Delta V$ | input transition rise and fall rate | | 0 | - | 10 | ns/V |
| T_{amb} | ambient temperature | in free air | -40 | - | +85 | °C |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ [1] | Max | Unit |
|---|---------------------------|--|----------------|----------------|------|------|
| $T_{amb} = -40$ °C to $+85$ °C | | | | | | |
| V_{IK} | input clamping voltage | $I_{IK} = -18$ mA; $V_{CC} = 2.7$ V | - | -0.9 | -1.2 | V |
| V_{OH} | HIGH-level output voltage | $I_{OH} = -100$ μ A; $V_{CC} = 2.7$ V to 3.6 V | $V_{CC} - 0.2$ | $V_{CC} - 0.1$ | - | V |
| | | $I_{OH} = -8$ mA; $V_{CC} = 2.7$ V | 2.4 | 2.5 | - | V |
| | | $I_{OH} = -32$ mA; $V_{CC} = 3.0$ V | 2.0 | 2.2 | - | V |

| Symbol | Parameter | Conditions | Min | Typ [1] | Max | Unit |
|-----------------------|------------------------------------|--|-----|---------|------|------|
| V _{OL} | LOW-level output voltage | V _{CC} = 2.7 V | | | | |
| | | I _{OL} = 100 μA | - | 0.1 | 0.2 | V |
| | | I _{OL} = 24 mA | - | 0.3 | 0.5 | V |
| | | V _{CC} = 3.0 V | | | | |
| | | I _{OL} = 16 mA | - | 0.25 | 0.4 | V |
| | | I _{OL} = 32 mA | - | 0.3 | 0.5 | V |
| I _I | input leakage current | all input pins | | | | |
| | | V _{CC} = 0 V or 3.6 V; V _I = 5.5 V | - | 1 | 10 | μA |
| | | control pins | | | | |
| | | V _{CC} = 3.6 V; V _I = V _{CC} or GND | - | ±0.1 | ±1 | μA |
| | | data pins [2] | | | | |
| | | V _{CC} = 3.6 V; V _I = V _{CC} | - | 0.1 | 1 | μA |
| I _{OFF} | power-off leakage current | V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V | - | 1 | ±100 | μA |
| | | V _{CC} = 3.6 V; V _I = 0 V | - | -1 | -5 | μA |
| I _{BHL} | bus hold LOW current | V _{CC} = 3 V; V _I = 0.8 V [3] | 75 | 150 | - | μA |
| I _{BHH} | bus hold HIGH current | V _{CC} = 3 V; V _I = 2.0 V | - | -150 | -75 | μA |
| I _{BHLO} | bus hold LOW overdrive current | V _{CC} = 3.6 V; V _I = 0 V to 3.6 V | 500 | - | - | μA |
| I _{BHHO} | bus hold HIGH overdrive current | V _{CC} = 3.6 V; V _I = 0 V to 3.6 V | - | - | -500 | μA |
| I _{LO} | output leakage current | output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 3.0 V | - | 60 | 125 | μA |
| I _{O(pu/pd)} | power-up/power-down output current | V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; nOE = don't care [4] | - | ±1 | ±100 | μA |
| I _{OZ} | OFF-state output current | V _{CC} = 3.6 V; V _I = V _{IH} or V _{IL} | | | | |
| | | output HIGH: V _O = 3.0 V | - | 1 | 5 | μA |
| | | output LOW: V _O = 0.5 V | - | -1 | -5 | μA |
| I _{CC} | supply current | V _{CC} = 3.6 V; V _I = GND or V _{CC} ; I _O = 0 A | | | | |
| | | outputs HIGH | - | 0.13 | 0.19 | mA |
| | | outputs LOW | - | 2 | 7 | mA |
| | | outputs disabled [5] | - | 0.13 | 0.19 | mA |
| ΔI _{CC} | additional supply current | per input pin; V _{CC} = 3 V to 3.6 V; one input at V _{CC} - 0.6 V and other inputs at V _{CC} or GND [6] | - | 0.1 | 0.2 | mA |
| C _I | input capacitance | V _I = 0 V or 3.0 V | - | 4 | - | pF |
| C _O | output capacitance | outputs disabled; V _O = 0 V or 3.0 V | - | 8 | - | pF |

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.

From V_{CC} = 1.2 V to V_{CC} = 3.0 V to 3.6 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.

[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

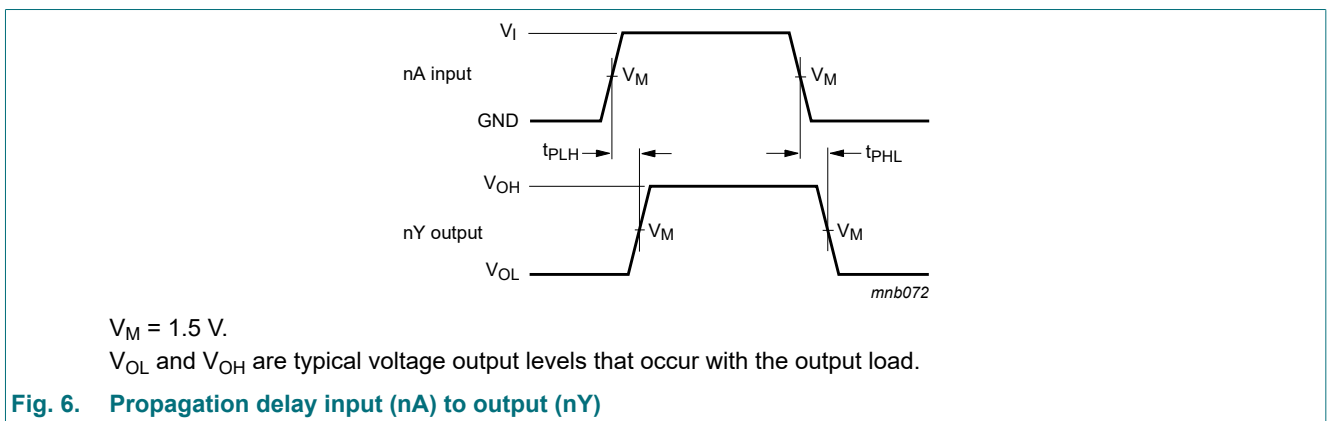
Table 7. Dynamic characteristics

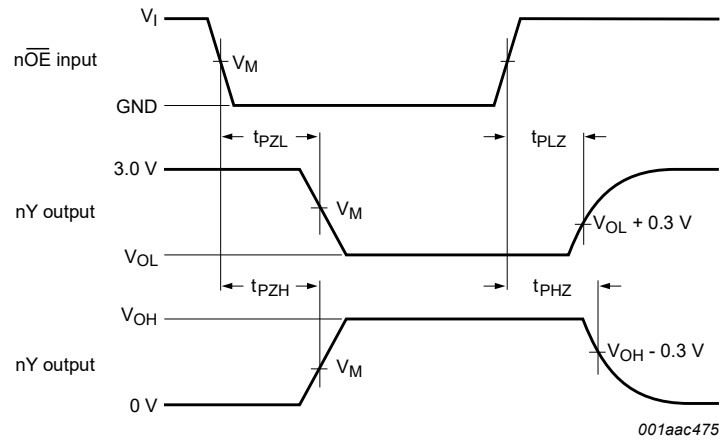
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

| Symbol | Parameter | Conditions | Min | Typ [1] | Max | Unit |
|---|-------------------------------------|--|-----|---------|-----|------|
| T_{amb} = -40 °C to +85 °C | | | | | | |
| t _{PLH} | LOW to HIGH propagation delay | nAn to nY; see Fig. 6 | | | | |
| | | V _{CC} = 2.7 V | - | - | 4.5 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.7 | 4.0 | ns |
| t _{PHL} | HIGH to LOW propagation delay | nAn to nY; see Fig. 6 | | | | |
| | | V _{CC} = 2.7 V | - | - | 4.9 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.9 | 3.9 | ns |
| t _{PZH} | OFF-state to HIGH propagation delay | n $\overline{\text{OE}}$ to nY; see Fig. 7 | | | | |
| | | V _{CC} = 2.7 V | - | - | 6.0 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 3.4 | 4.7 | ns |
| t _{PZL} | OFF-state to LOW propagation delay | n $\overline{\text{OE}}$ to nY; see Fig. 7 | | | | |
| | | V _{CC} = 2.7 V | - | - | 6.5 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.1 | 3.4 | 4.7 | ns |
| t _{PHZ} | HIGH to OFF-state propagation delay | n $\overline{\text{OE}}$ to nY; see Fig. 7 | | | | |
| | | V _{CC} = 2.7 V | - | - | 5.7 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.8 | 3.7 | 5.1 | ns |
| t _{PLZ} | LOW to OFF-state propagation delay | n $\overline{\text{OE}}$ to nY; see Fig. 7 | | | | |
| | | V _{CC} = 2.7 V | - | - | 4.0 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.3 | 2.6 | 4.5 | ns |

[1] Typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

10.1. Waveforms and test circuit

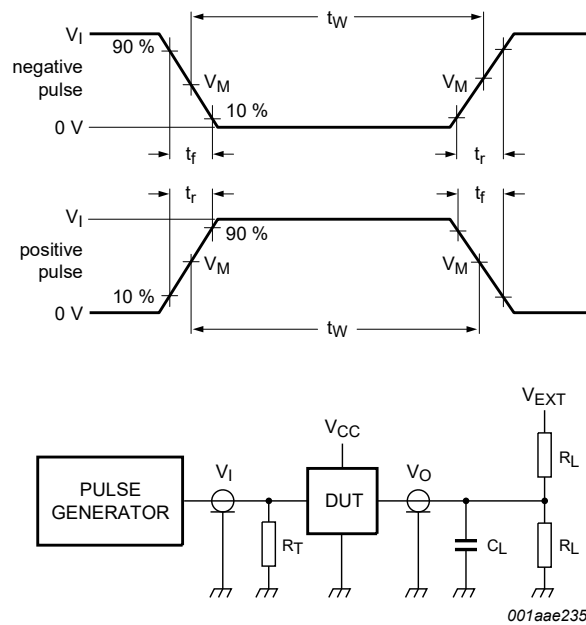




$V_M = 1.5 V$.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Enable and disable times of 3-state outputs



Test data is given in [Table 8](#).

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Fig. 8. Test circuit for measuring switching times

Table 8. Test data

| Input | | | | Load | | V_{EXT} | | |
|-------|---------------|--------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| V_I | f_i | t_w | t_r, t_f | C_L | R_L | t_{PHZ}, t_{PZH} | t_{PLZ}, t_{PLZ} | t_{PLH}, t_{PHL} |
| 2.7 V | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | GND | 6 V | open |

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

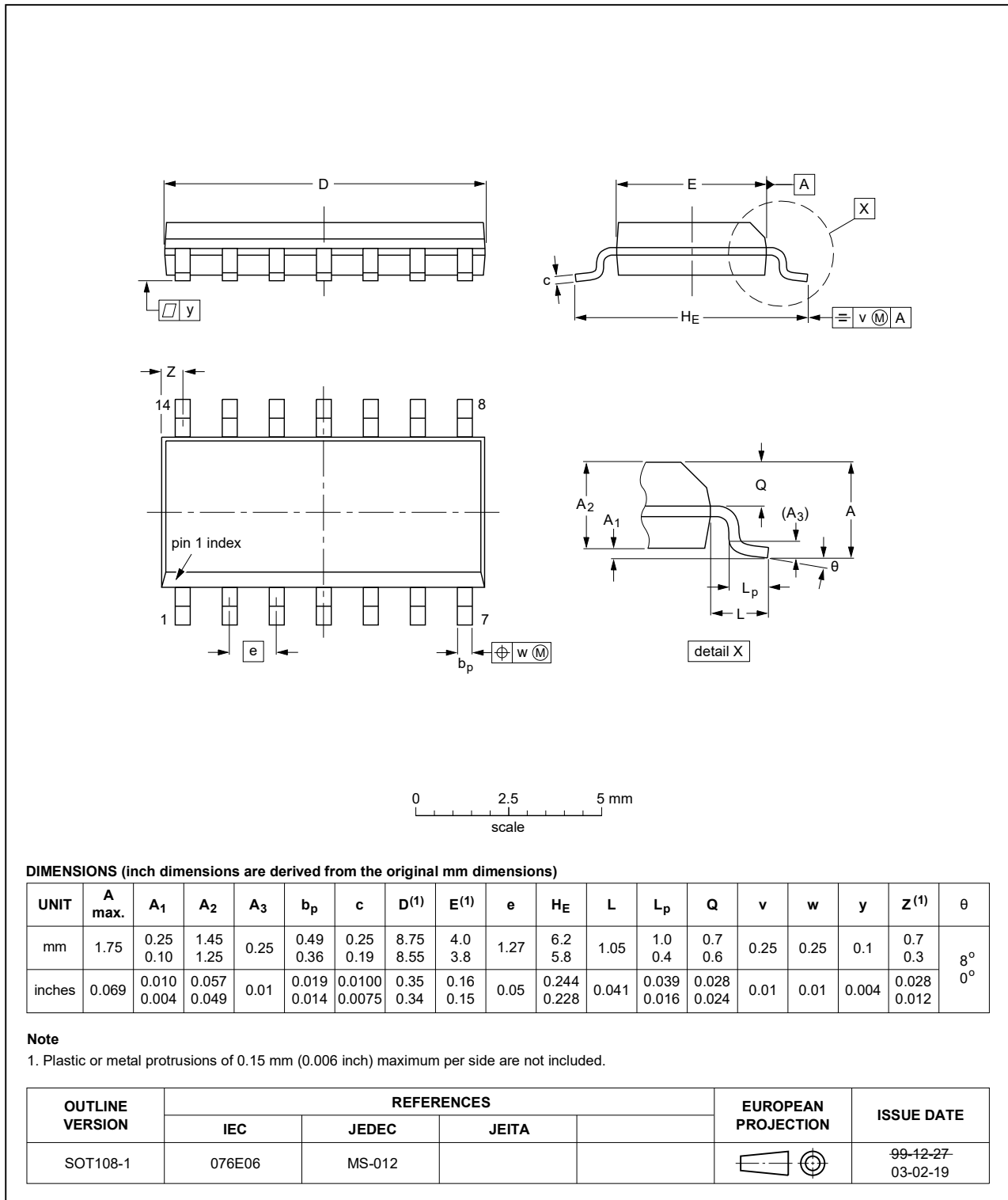


Fig. 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

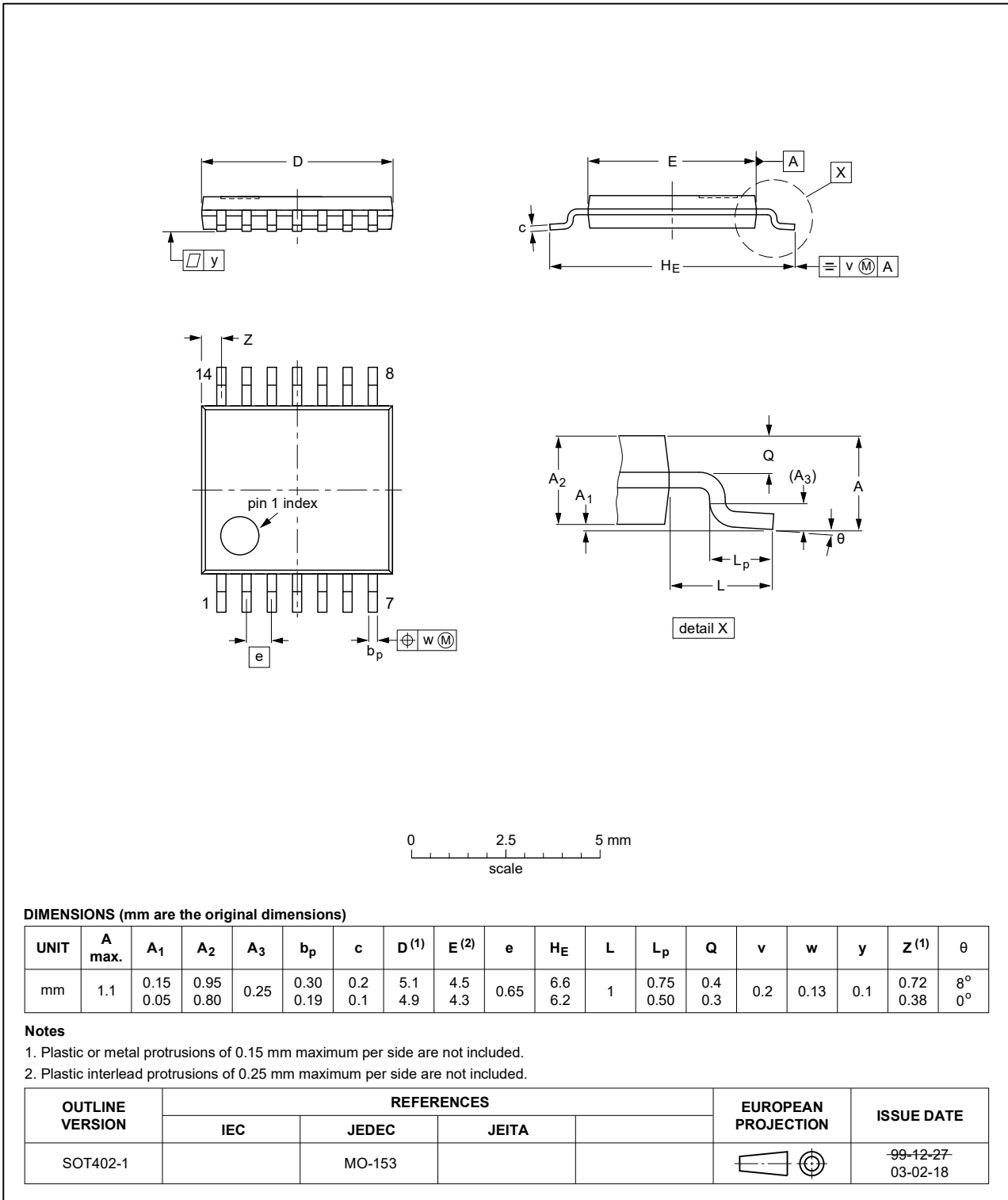


Fig. 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

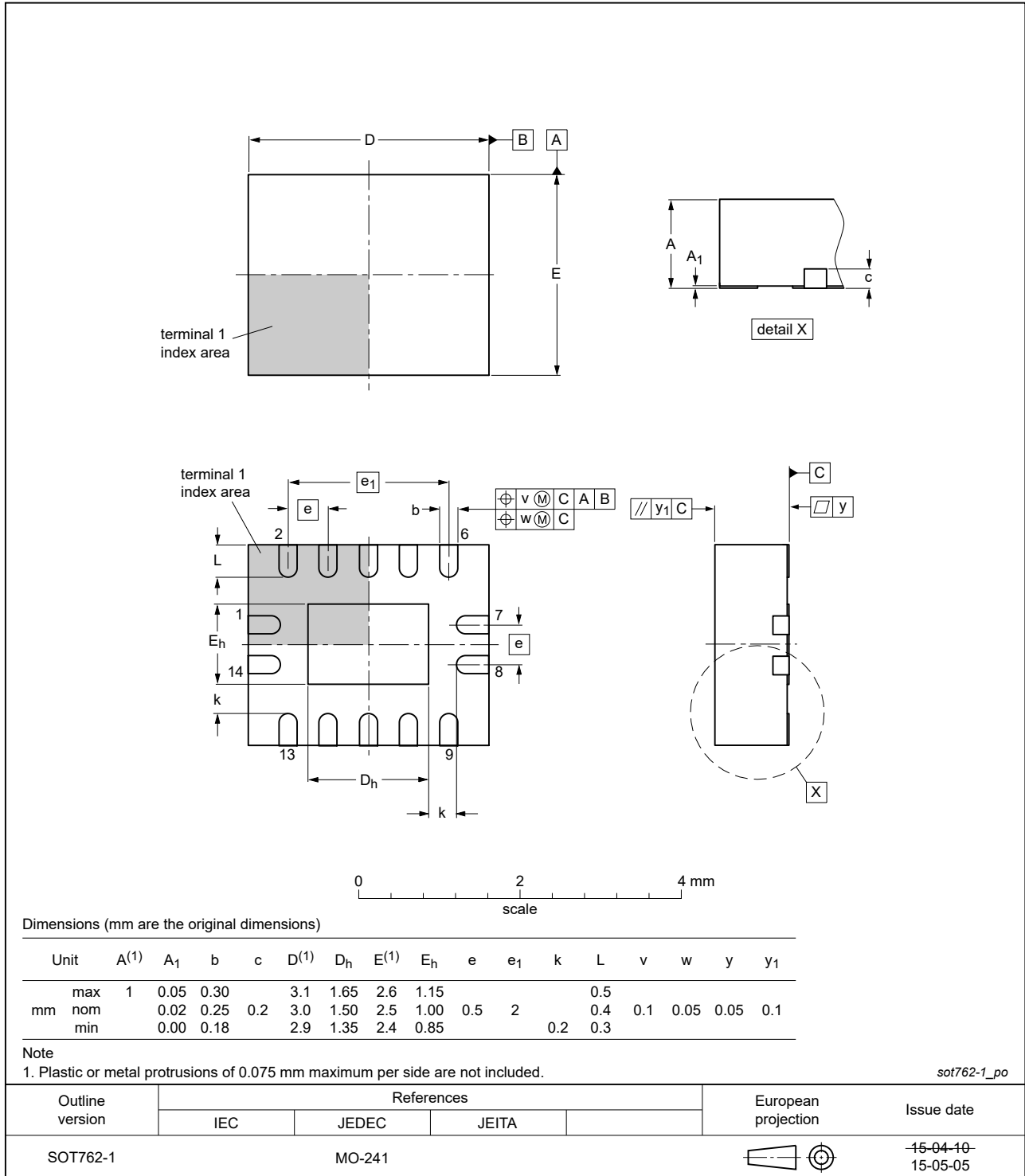


Fig. 11. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 9. Abbreviations

| Acronym | Description |
|---------|---|
| BiCMOS | Bipolar Complementary Metal Oxide Semiconductor |
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|--|-----------------------|---------------|-------------------|
| 74LVT_LVTH125 v.8 | 20210818 | Product data sheet | - | 74LVT_LVTH125 v.7 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74LVT125DB and 74LVTH125DB (SOT337-1/SSOP14) removed. Section 1 and Section 2 updated. Fig. 7 aligned with test conditions (errata). | | | |
| 74LVT_LVTH125 v.7 | 20160531 | Product data sheet | - | 74LVT125 v.6 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. | | | |
| 74LVT_LVTH125 v.6 | 20060306 | Product data sheet | - | 74LVT125 v.5 |
| Modifications: | <ul style="list-style-type: none"> Section 3: Added type numbers 74LVTH125D, 74LVTH125DB, 74LVTH125PW and 74LVTH125BQ. | | | |
| 74LVT125 v.5 | 20050210 | Product data sheet | - | 74LVT125 v.4 |
| 74LVT125 v.4 | 20050207 | Product data sheet | - | 74LVT125 v.3 |
| 74LVT125 v.3 | 20040624 | Product data sheet | - | 74LVT125 v.2 |
| 74LVT125 v.2 | 19980219 | Product specification | - | 74LVT125 v.1 |
| 74LVT125 v.1 | - | - | - | - |

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| Document status [1][2] | Product status [3] | Definition |
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Contents

| | |
|--|-----------|
| 1. General description | 1 |
| 2. Features and benefits | 1 |
| 3. Ordering information | 1 |
| 4. Functional diagram | 2 |
| 5. Pinning information | 2 |
| 5.1. Pinning..... | 2 |
| 5.2. Pin description..... | 3 |
| 6. Functional description | 3 |
| 7. Limiting values | 4 |
| 8. Recommended operating conditions | 4 |
| 9. Static characteristics | 4 |
| 10. Dynamic characteristics | 6 |
| 10.1. Waveforms and test circuit..... | 6 |
| 11. Package outline | 8 |
| 12. Abbreviations | 11 |
| 13. Revision history | 11 |
| 14. Legal information | 12 |

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